We claim:

1. A memory device comprising:

a first input/output conductor formed above or on a first plane of a substrate;

a second input/output conductor;

a semiconductor region located between said first input/output conductor and said second input/output conductor an intersection of their projections;

a charge storage medium; and

wherein charge stored in said charge storage medium affects the amount of current that flows between said first input/output conductor and second input/output conductor.

2. The memory device of claim 1 wherein said charge storage medium is formed between the intersection of said first input/output conductor and said second input/output conductor.

3. The memory device of claim 2 wherein said charge storage medium is formed directly on said semiconductor region.

4. The memory device of claim 1 wherein said charge storage medium is formed adjacent to said semiconductor region.

5. The memory of claim 4 further comprising a control gate formed adjacent to said charge storage medium.

6. The memory of claim 1 wherein current flows through said semiconductor region in a direction perpendicular to said plane of said substrate.

7. The memory of claim 1 wherein said semiconductor region comprises doped silicon.

8. A memory device comprising:

a first input/output conductor formed above or on a first plane of a substrate;

a second input/output conductor formed above said first input/output conductor and having a projected intersection with said first input/output conductor;

a silicon body located between said first input/output conductor and said second input/output conductor and in direct alignment with said intersection of said first and second input/output conductors;

a charge storage medium; and

wherein read current flows through said silicon body between said first input/output and said second input/output in a direction perpendicular to the plane of said substrate and wherein charge stored in said charge storage medium affects the amount of read current that flows between said first input/output conductor and said second input/output conductor for a given voltage applied between said first input/output conductor and said second input/output conductor.

9. The memory device of claim 8 wherein said charge storage medium is formed on said silicon body and in direct alignment with said intersection of said first and said second input/output conductors.

10. The memory device of claim 8 wherein said charge storage medium is formed adjacent to said silicon body.

11. The memory device of claim 8 further comprising a control gate formed adjacent to said charge storage medium.

12. A memory device comprising:

a first input/output conductor formed above or on a first plane of a substrate;

a second input/output conductor formed above the first input/output conductor;

a third input/output conductor formed above the second input/output conductor;

a first semiconductor region located between an intersection of projections of said first input/output conductor and said second input/output conductor;

a second semiconductor region located between an intersection of projections of said second input/output conductor and said third input/output conductor; and

a first charge storage medium that affects the amount of current that flows between said first input/output conductor and second input/output conductor.

13. A memory cell comprising:

a diode having a first region and a second region;

a charge storage region;

an insulation region disposed adjacent to the charge storage region;

a first contact to the first region, and

a second contact;

wherein a predetermined potential across the first and second contacts causes a current to flow through the diode, insulation region and charge storage region.

14. The memory cell of claim 13 including a second insulation region disposed adjacent the second contact and the storage region opposing to the first insulation region.

15. The memory cell of claim 13 wherein the insulation regions are oxide regions.

16. The memory cell of claim 13 wherein the storage region includes a nitrogen compound.

17. The memory cell of claim 16 wherein the compound includes oxygen.

18. The memory cell of claim 16 wherein the compound includes silicon.

19. The memory cell of claim 16 wherein the storage region comprises alumina.

20. The memory cell of claim 13 wherein the diode comprises doped substrate regions.

21. The memory cell of claim 14 wherein the diode comprises layers disposed above a substrate.

22. The memory cell of claim 15 wherein the oxide regions are approximately 1-5nm thick.

23. The memory cell of claim 22 wherein the oxide region is approximately 2-3nm thick.

24. A nonvolatile read-write memory cell comprising:

an N doped region;

a P doped region;

a storage element disposed between the N doped region and the P doped region;

conductors for passing a current through the N doped region, the P doped region and the storage element.

25. The memory cell defined by claim 24 wherein the storage element comprises a first oxide region.

26. The memory cell defined by claim 25 wherein the storage element comprises a second oxide region.

27. The memory cell defined by claim 25 wherein the storage element comprises a region containing nitrogen.

28. The memory cell defined by claim 27 wherein the storage element comprises a second oxide region.

29. The memory cell defined by claim 24 wherein the storage element is in direct electrical contact with at least one of the doped regions.

30. The memory cell defined by claim 24 wherein the storage element includes silicon.

31. The memory cell defined by claim 25 wherein the storage element comprises alumina.

32. The memory cell defined by claim 24 wherein at least one of the doped regions is disposed in a substrate.

33. The memory cell defined by claim 24 wherein at least one of the doped regions is disposed above a substrate.

34. A method for operating a memory cell comprising:
trapping charge in a region to program the cell;
passing a current through the region when reading data from the cell.

35. The method defined by claim 34 where the passing step includes causing a current to flow in a first direction to program and read the cell.

36. The method defined by claim 34 where the passing step further includes causing a current to flow in a second direction to erase the cell.

37. The method defined by claim 34 wherein the trapping step includes passing a current through a storage element in a first direction.

38. The method defined by claim 34 wherein the erasing step includes passing current through a storage element in a second direction.

39. In a structure having a diode and an oxide region that exhibits a negative-resistance characteristic as a voltage forward biases the diode, an improvement comprising:

a storage region for trapping charge disposed adjacent to the oxide region such that a current through the diode and oxide region passes through the storage region.

40. The improved structure defined by claim 39 wherein the storage region comprises a compound that includes nitrogen.

41. The improved structure defined by claim 40 wherein the compound includes oxygen.

42. The improved structure defined by claim 41 wherein the compound includes silicon.

43. The improved structure defined by claim 39 wherein the storage region comprises alumina.

44. An array of memory cells comprising:

a plurality of cells having at least one semiconductor region and a storage region for trapping charge; and

a control means for controlling the flow of current through the semiconductor region and the storage region.

45. The array defined by claim 44 wherein the control means is disposed in the cells.

46. The array defined by claim 44 wherein the at least one semiconductor region is N type.

47. The array defined by claim 46 wherein the control means comprises a P type semiconductor region and is disposed adjacent the N type semiconductor region.

48. The array defined by claim 47 wherein the storage means includes an oxide region.

49. The array defined by claim 48 wherein the storage means includes a nitrogen compound.

50. The array defined by claim 44 wherein the control means is disposed externally to the cells.

51. The array defined by claim 44, wherein the semiconductor regions of the cells are disposed in a substrate.

52. The array defined by claim 44 wherein semiconductor regions of the cells are formed of polysilicon.

53. The array defined by claim 47 wherein the control means comprises an n-channel, field-effect transistor which includes the n-type region.

54. A memory array having N levels where N is two or more, fabricated above a substrate, each level comprising:

first spaced-apart conductors in a first plane parallel to the substrate;

second spaced-apart conductors in a second plane parallel to the substrate and above the first plane;

a plurality of cells one disposed between each of the first and second conductors, each cell comprising:

a steering element which more readily conducts current in one direction, and

a storage stack comprising first and second oxide regions with a storage region between the oxide regions;

the steering element and storage stack being disposed between the first and second conductors such that a current from one conductor passes through the steering element, first oxide, storage region and second oxide before reaching the second conductor.

55. The memory array defined by claim 54 wherein the second conductors in a level N-1 are shared with cells above and below the second conductors.

56. The memory array defined by claim 54 wherein the steering element comprises a p-type region and an n-type region with the storage stack being in contact with at least the n-type doped region.

57. In a three dimensional memory array having a plurality of levels disposed above a substrate, each level having nonlinear elements, an improvement comprising:

a storage stack associated with each of the nonlinear elements comprising a storage region for trapping charge disposed between regions of oxide such that a current flowing through the nonlinear elements passes through one of the oxide regions, the storage region and the other oxide region.

58. The improvement defined by claim 57 wherein charge is trapped in the storage region by passing a current of at least a first predetermined density in a first direction.

59. The improvement defined by claim 58 wherein charge trapped in the storage region is sensed by passing a current in the first direction of less than a second predetermined density, said second density being less than the first density.

60. The improvement defined by claim 59 wherein trapped charge is neutralized by a current through the storage region in a second direction opposite to the first direction.

61. The improvement defined by claim 60 wherein when the current passes in the first direction the diodes are forward biased.

62. The improvement defined by claim 61 wherein the storage region includes a compound of nitrogen.

63. The improvement defined by claim 62 wherein the diode includes an n-type semiconductor region adjacent to one of the oxide regions.

64. A memory comprising:

a single crystalline substrate having a plane;

a first contact on or above said plane of said substrate;

a body on said first contact;

a second contact on said body wherein said second contact is substantially vertically aligned over said first contact;

a charge storage medium adjacent to said wherein read current flows between said first contact and said second contact in a direction perpendicular to said plane of said substrate; and

a control gate adjacent to said charge storage medium.

65. The memory of claim 64 wherein said body comprises silicon.

66. The memory of claim 64 wherein said body comprises a dielectric film surrounded by a silicon film.

67. The memory of claim 64 wherein said charge storage medium comprises a dielectric stack.

68. The memory of claim 64 wherein said charge storage medium comprises a silicon floating gate separated from said body by a dielectric.

69. The memory of claim 64 wherein said charge storage medium comprises a floating gate formed from conductive nanocrystals and separated from said body by a dielectric.

70. A memory comprising:

a silicon crystal substrate having a plane;

a first silicon film having a first conductivity type and a first concentration of said first conductivity type dopants formed above said substrate;

a second silicon film having a second conductivity type and a second concentration of said second conductivity type dopants, wherein said first concentration is greater than said second concentration;

a third silicon film having said first conductivity type and a third concentration of said first conductivity type dopants, wherein said first silicon film and said third silicon film are substantially vertically aligned;

a charge storage medium adjacent to said second silicon film; and

a control gate adjacent to said charge storage medium.

71. The memory of claim 70 wherein said charge storage medium comprises an ONO film.

72. The memory of claim 70 wherein said charge storage medium comprises a first dielectric layer adjacent to said second silicon film, a floating gate adjacent to said first dielectric layer, and a second dielectric layer between said floating gate and said control gate.

73. The memory of claim 72 wherein said floating gate comprises nanocrystals.

74. The memory of claim 72 wherein said floating gate comprises a continuous silicon film.

75. The memory of claim 70 wherein said first conductivity type is N type conductivity and wherein said second conductivity type is P type conductivity.

76. A memory comprising:

a first metal contact formed above a substrate;

a silicon film having a first conductivity type formed on said first metal contact and forming a Schottky junction with said first metal contact;

a second metal contact formed on said silicon film and forming a second Schottky junction with said silicon film;

a charge storage medium adjacent to said silicon film; and

a control gate adjacent to said charge storage medium.

77. The memory of claim 76 wherein said charge storage medium comprises an ONO film.

78. The memory of claim 76 wherein said charge storage medium comprises a first dielectric adjacent to said silicon film, a floating gate adjacent to said first dielectric and a second dielectric between said floating gate and said control gate.

79. The memory of claim 78 wherein said floating gate comprises nanocrystals.

80. The memory of claim 78 wherein said floating gate is a silicon floating gate.

81. The memory of claim 78 wherein said first conductivity type is P type conductivity.

82. A memory comprising:

a first silicon film having a first conductivity type formed above a substrate;

a first dielectric layer formed on said first silicon film;

a second silicon film of said first conductivity type formed on dielectric layer;

a third silicon film adjacent to and in contact with said first silicon film, said first dielectric layer and said second silicon film, wherein said third silicon film has a second conductivity type opposite said first conductivity type;

a charge storage medium adjacent to said third silicon film; and

a control gate adjacent to said charge storage medium.

83. The memory of claim 82 wherein said charge storage medium is an ONO film.

84. The memory of claim 82 wherein said charge storage medium comprises a third dielectric adjacent to said third silicon film, a floating gate

adjacent to said second dielectric and a third dielectric between said floating gate and said control gate.

85. The memory of claim 84 wherein said floating gate is formed from nanocrystals.

86. The memory device of claim 84 wherein said floating gate is formed from silicon.

87. The memory device of claim 82 wherein said first conductivity type is N type conductivity type and wherein said second conductivity type is P type conductivity.

88. A memory comprising:

a substrate;

a first silicon film having a first conductivity type and a first concentration of said first conductivity type over said substrate;

a second silicon film having a second concentration of said first conductivity type on said first silicon film wherein said second concentration is less than said first concentration;

a third silicon film having a second conductivity type formed on said second silicon film;

a charge storage medium adjacent to said second silicon film; and

a control gate adjacent to said charge storage medium.

89. The memory of claim 88 wherein said charge storage medium comprises an ONO film.

90. The memory of claim 88 wherein said charge storage device comprises a first dielectric adjacent to said second silicon film, a floating gate adjacent to said first dielectric and a second dielectric between said floating gate and said control gate.

91. The memory device of claim 90 wherein said floating gate is formed from nanocrystals.

92. The memory of claim 90 wherein said floating gate is formed from silicon.

93. The memory of claim 88 wherein said first conductivity type is P type conductivity and wherein said second conductivity type is N type conductivity.

94. A memory comprising:

a single crystal silicon substrate having a plane;

a dielectric formed above said plane of said single crystal silicon substrate;

a first contact formed on said dielectric;

a body formed on said first contact;

a second contact formed on said body;

a charge storage medium adjacent to said body and wherein read current flows between said first contact and said second contact in a direction perpendicular to said plane of said substrate; and

a control gate adjacent to said charge storage medium.

95. A memory comprising:

a first pillar comprising a first contact, a body on said first contact, and a second contact on said body;

a second pillar formed above said first pillar said second pillar comprising a third contact, a second body formed on said third contact and a fourth contact formed on said second body;

a first charge storage medium adjacent to said first pillar;

a second charge storage medium adjacent to said second pillar; and

a continuous film control gate formed adjacent to said first charge storage medium and said second charge storage medium.

96. The memory of claim 95 wherein said first charge storage medium comprise a film containing nanocrystals.

97. A memory comprising:

a first pillar comprising a first contact, a body on said first contact, and a second contact on said body;

a second pillar formed above said first pillar said second pillar comprising a third contact, a second body formed on said third contact and a fourth contact formed on said body;

a first dielectric formed on the sidewalls of said first pillar and said second pillar;

a nanocrystals film formed on and adjacent to said first dielectric adjacent to said first and second pillars;

a second dielectric formed adjacent to said nanocrystals;

a first control gate formed adjacent to said second dielectric adjacent to said first pillar; and

a second control gate formed adjacent to said second dielectric adjacent to said second pillar.

98. The memory of claim 97 wherein said first control gate and said second control gate are formed from a continuous film.

99. A semiconductor device comprising:

a monolithic three dimensional array of charge storage devices formed in an amorphous or polycrystalline semiconductor layer over a monocrystalline semiconductor substrate; and

driver circuitry formed in the substrate at least in part under the array, within the array or above the array.

100. The semiconductor device of claim 99, wherein the driver circuitry comprises at least one of sense amps and charge pumps formed under the array in the substrate.

101. The semiconductor device of claim 99, wherein at least one surface between two successive device levels is planarized by chemical mechanical polishing.

102. The semiconductor device of claim 101, wherein the array contains four or more device levels.

103. The semiconductor device of claim 102 wherein each charge storage device is selected from a group consisting of a pillar TFT EEPROM, a

pillar diode with a charge storage region, a self aligned TFT EEPROM, and a rail stack TFT EEPROM.

104. The semiconductor device of claim 103, wherein each level of array is separated from another level of the array by a polished planar interlayer insulating layer.

105. The semiconductor device of claim 104, wherein each device level is planar with respect to the adjacent device levels.

106. A three dimensional semiconductor device comprising a plurality of device levels, each level contains:

an active semiconductor region;

a charge storage region;

a first electrode;

a second electrode; and

wherein a first side of the active semiconductor region is aligned to a first side of one of the first and the second electrodes.

107. The semiconductor device of claim 106, wherein a second side of the active semiconductor region is aligned to a second side of the other one of the first and the second electrodes.

108. The semiconductor device of claim 107, wherein:

the active semiconductor region comprises a vertical pillar including a channel, a source and a drain region;

the first and the second electrodes contact one of the source and the drain regions; and

the device further comprises a gate electrode.

109. The semiconductor device of claim 107, wherein:

the active semiconductor region comprises a vertical p-n junction pillar; and

the first and the second electrodes contact one of the p and the n regions of the p-n junction.

110. A method of making a three dimensional semiconductor device comprising a plurality of device levels, the method of making each device level comprises:

forming an active semiconductor region;

forming a charge storage region;

forming a first electrode;

forming a second electrode; and

patterning at least two sides of the active semiconductor region and a first electrode during a same photolithography step.

111. The method of claim 110, wherein the active semiconductor region and a first electrode are etched using a first mask.

112. The method of claim 111, further comprising etching the second electrode and the active semiconductor region using a second mask.

113. The method of claim 111, wherein:

the active semiconductor region comprises a vertical pillar including a channel, a source and a drain region;

the first and the second electrodes contact one of the source and the drain regions; and

further comprising forming a gate electrode.

114. The method of claim 111, wherein:

the active semiconductor region comprises a vertical p-n junction pillar; and

the first and the second electrodes contact one of the p regions and the n regions of the p-n junction.

115. A semiconductor device comprising:

an active semiconductor region containing a channel, a source and a drain region;

a gate insulating layer;

a source electrode;

a drain electrode; and

a gate electrode;

wherein a first side of the active semiconductor region is aligned to a side of the gate electrode only in the channel portion of the active semiconductor region.

116. The device of claim 115, wherein the gate insulating layer comprises a portion of a charge storage region.

117. The device of claim 116, wherein the device comprises a self aligned TFT incorporated into a monolithic three dimensional array of devices.

118. A method of making a semiconductor device, comprising:

forming an active semiconductor region containing a channel, a source and a drain region;

forming a gate insulating layer;

forming a source electrode;

forming a drain electrode;

forming a gate layer; and

patterning the gate layer and the source and drain regions but not the channel region of the active semiconductor layer during a same photolithography step.

119. The method of claim 118, wherein:

the active semiconductor region and a gate layer are etched using a first mask; and

the gate insulating layer comprises a portion of a charge storage region.

120. The method of claim 119, further comprising forming a monolithic three dimensional array of charge storage devices, which includes the patterned active semiconductor layer.

121. A field effect transistor, comprising:

a source;

a drain;

a channel;

a gate;

at least one insulating layer between the gate and the channel; and

a gate line which extends substantially parallel to a source-channel-drain direction and which contacts the gate and is self aligned to the gate.

122. The transistor of claim 121, wherein the source, the drain and the channel are formed in a polysilicon active layer, which is located above an interlayer insulating layer.

123. The transistor of claim 122, wherein:

the transistor comprises an EEPROM;

the gate comprises a control gate; and

the at least one insulating layer is located in a charge storage region between the control gate and the channel.

124. The transistor of claim 123, wherein the charge storage region comprises an ONO dielectric film or an insulating layer containing conductive nanocrystals.

125. The transistor of claim 123, wherein the charge storage region comprises:

a tunnel dielectric above the channel;

a floating gate above the tunnel dielectric; and

a control gate dielectric above the floating gate.

126. The transistor of claim 123, further comprising:

sidewall spacers located adjacent to gate sidewalls and having approximately the same height as the gate; and

an intergate insulating layer which is located adjacent to the sidewall spacers and above the source and drain regions, and which has approximately the same height as the sidewall spacers.

127. The transistor of claim 126, wherein:

the gate line is located above the sidewall spacers and the intergate insulating layer; and

the gate line contacts the gate through an opening between the sidewall spacers.

128. The transistor of claim 127, further comprising:

a first bit line contacting the source region; and

a second bit line contacting the drain region;

wherein the first and the second bit lines are located under the intergate insulating layer, and extend in a direction substantially perpendicular to the source-channel-drain direction.

129. The transistor of claim 124, wherein the gate comprises:

a first portion contacting the charge storage region; and

a second portion above the first portion;

wherein the first and the second gate portions comprise separately deposited layers.

130. The transistor of claim 126, wherein:

the gate line comprises a word line comprising a silicide layer between two polysilicon layers; and

the gate line is located directly on the intergate insulating layer and top portions of the sidewall spacers.

131. The transistor of claim 123, wherein the gate line comprises a word line which is self aligned to the channel and the charge storage region.

132. A three dimensional nonvolatile device array, comprising:

a plurality of vertically separated device levels, each level comprising an array of TFT EEPROMs, each TFT EEPROM comprising a channel, source and drain regions, and a charge storage region adjacent to the channel region;

a plurality of bit line columns in each device level, each bit line contacting the source or the drain regions of the TFT EEPROMs;

a plurality of word line rows in each device level; and

at least one interlayer insulating layer located between the device levels.

133. The array of claim 132, wherein:

in at least one device level, the bit line columns are disposed on an opposite side of TFT EEPROM channels from the word line rows;

the channel of each TFT EEPROM comprises amorphous silicon or polysilicon;

the columns of bit lines extend substantially perpendicular to a source-channel-drain direction of the TFT EEPROMs;

each word line contacts the control gates of the TFT EEPROMs or each word line acts as a control gate of the TFT EEPROMs, and the rows of word lines extend substantially parallel to the source-channel-drain direction of the TFT EEPROMs; and

word lines are self aligned to the control gates of the array of TFT EEPROMs and the word lines are self aligned to the channel and the

charge storage regions of the TFT EEPROMs located below the respective word lines.

134. The array of claim 133, wherein each charge storage region comprises an ONO dielectric film or an insulating layer containing conductive nanocrystals.

135. The array of claim 133, wherein each charge storage region comprises:

a tunnel dielectric above the channel;

a floating gate above the tunnel dielectric; and

a control gate dielectric above the floating gate.

136. The array of claim 133, further comprising:

sidewall spacers located adjacent to sidewalls of the control gates of the TFT EEPROMs, wherein the sidewall spacers have approximately the same height as the control gates; and

an intergate insulating layer which is located between the sidewall spacers above the source and drain regions of the TFT EEPROMs in each device layer, and wherein the intergate insulating layer has approximately the same height as the sidewall spacers.

137. The array of claim 136, wherein:

the word lines are located on the sidewall spacers and on the intergate insulating layer in each device level; and

the word lines contact the respective TFT EEPROM control gates through an opening between the sidewall spacers.

138. The array of claim 137, wherein the bit lines in each device level comprise rails which extend under the intergate insulating layer.

139. The array of claim 138, wherein:

the rails comprise silicide layers over doped semiconductor regions; and

the doped semiconductor regions comprise the TFT EEPROM source and drain regions in areas where the doped semiconductor regions are located adjacent to the TFT EEPROM channels.

140. The array of claim 132, wherein each control gate comprises:

a first portion contacting the charge storage region; and

a second portion above the first portion;

wherein the first and the second gate portions comprise separately deposited layers.

141. The array of claim 132, further comprising word line contacts and bit line contacts which connect the word lines and the bit lines with peripheral circuits located in a semiconductor substrate below the first device level of the array.

142. The array of claim 141, wherein the word line and the bit line contacts extend between plural device layers.

143. The array of claim 132, wherein:

each memory cell comprises a TFT EEPROM; and

each memory cell size per bit is about $(2F^2)/N$, where F is a minimum feature size and N is a number of device layers in a third dimension and where $N>1$.

144. An EEPROM comprising:

a channel;

a source;

a drain;

a tunneling dielectric located above the channel;

a floating gate located above the tunneling dielectric;

sidewall spacers located adjacent to the floating gate sidewalls;

a word line located above the floating gate; and

a control gate dielectric located between the control gate and the floating gate;

wherein the control gate dielectric is located above the sidewall spacers.

145. The EEPROM of claim 144, wherein:

the sidewall spacers extend to a top of the floating gate; and

the control gate dielectric is located on top surfaces of the floating gate and the sidewall spacers.

146. The EEPROM of claim 144, wherein the floating gate extends vertically above the sidewall spacers.

147. The EEPROM of claim 146, wherein the floating gate extends laterally above the sidewall spacers, such that the floating gate has a "T" shape.

148. The EEPROM of claim 147, wherein:

the control gate dielectric is located over a top surface and side surfaces of the floating gate which extend above the sidewall spacers; and

the word line is located over the control gate dielectric, such that the word line acts as a control gate of the EEPROM.

149. The EEPROM of claim 146, wherein a top surface of the floating gate is roughened or textured.

150. The EEPROM of claim 144, wherein the source, the drain and the channel are formed in a polysilicon active layer, which is located above an interlayer insulating layer, such that the EEPROM comprises a TFT.

151. A three dimensional memory array, comprising:

a plurality of vertically separated device levels, each level comprising an array of TFT EEPROMs of claim 150;

a plurality of bit line columns in each device level, each bit line contacting the source or the drain regions of the TFT EEPROMs, and the columns of bit lines extending substantially perpendicular to a source-channel-drain direction of the TFT EEPROMs;

a plurality of word line rows in each device level, and the rows of word lines extending substantially parallel to the source-channel-drain direction of the TFT EEPROMs; and

at least one interlayer insulating layer located between the device levels.

152. The array of claim 150, wherein:

the word lines are self aligned to the channels and the floating gates of the TFT EEPROMs; and

the bit lines in each device level comprise rails which extend under the word lines.

153. An array of nonvolatile memory cells, wherein each memory cell comprises a semiconductor device and each memory cell size per bit is about $(2f^2)/N$, where f is a minimum feature size and N is a number of device layers in a third dimension, and where $N \geq 1$.

154. The array of claim 153, wherein:

the array comprises a monolithic three dimensional memory array, comprising a plurality of vertically separated device levels, where $N > 1$; and

the semiconductor device comprises a TFT EEPROM comprising a channel, source and drain regions, and a charge storage region.

155. The array of claim 154, further comprising:

a plurality of bit line columns in each device level, each bit line contacting the source or the drain regions of the TFT EEPROMs, and the columns of the bit lines extending substantially perpendicular to a source-channel-drain direction of the TFT EEPROMs;

a plurality of word line rows in each device level, and the rows of the words lines extending substantially parallel to the source-channel-drain direction of the TFT EEPROMs; and

at least one interlayer insulating layer located between the device levels.

156. The array of claim 155, wherein:

the TFT EEPROMs further comprise control gates; and

the plurality of word lines are self aligned to the control gates of the respective TFT EEPROMs, to the channel regions of the respective TFT EEPROMs, and to the charge storage regions of the respective TFT EEPROMs located below the respective word lines.

157. The array of claim 156, wherein the TFT EEPROMs further comprise:

sidewall spacers located adjacent to sidewalls of the gates of the TFT EEPROMs, wherein the sidewall spacers have approximately the same height as the gates; and

an intergate insulating layer which is located between the sidewall spacers, and above the source and the drain regions of the TFT EEPROMs in each device layer, and wherein the intergate insulating layer has approximately the same height as the sidewall spacers.

158. The array of claim 157, wherein:

the word lines are located on the sidewall spacers and on the intergate insulating layer in each device level; and

the word lines contact the respective TFT EEPROM control gates through an opening between the sidewall spacers.

159. The array of claim 155, wherein the TFT EEPROMs further comprise: floating gates located in the charge storage regions;

sidewall spacers located adjacent to sidewalls of the floating gates of the TFT EEPROMs; and

an intergate insulating layer which is located between the sidewall spacers, and above the source and the drain regions of the TFT EEPROMs in each device layer, and wherein the intergate insulating layer has approximately the same height as the sidewall spacers; and

a control gate dielectric located above the sidewall spacers and the intergate insulating layer and below the word lines.

160. The array of claim 159, wherein the floating gates extend vertically and laterally above the sidewall spacers, such that the floating gates have a "T" shape.

161. The array of claim 155, further comprising word line contacts and bit line contacts which connect the word lines and the bit lines with peripheral circuits located in a semiconductor substrate below the first device level of the array; and

wherein the bit line contacts extend between plural device layers.

162. A method of making an EEPROM, comprising:

providing a semiconductor active area;

forming a charge storage region over the active area;

forming a conductive gate layer over the charge storage region;

patterning the gate layer to form a control gate overlying the charge storage region;

doping the active area using the control gate as a mask to form source and drain regions in the active area;

forming a first insulating layer above and adjacent to the control gate;

exposing a top portion of the control gate without photolithographic masking; and

forming a word line contacting the exposed top portion of the control gate, such that the word line is self aligned to the control gate.

163. The method of claim 162, further comprising:

forming a blocking layer above the gate layer;

patterning the blocking layer during the step of patterning the gate layer;

forming sidewall spacers adjacent to the control gate and the blocking layer sidewalls.

164. The method of claim 163, wherein:

the blocking layer comprises a different material than a material of the sidewall spacers and a material of the control gate;

the step of exposing the top portion of the control gate comprises planarizing the first insulating layer to expose the blocking layer and selectively removing the blocking layer from between the sidewall spacers to form a gate contact via; and

the step of forming a word line comprises depositing the word line over the first insulating layer and in the gate contact via, such that the portion of the word line in the gate contact via forms a top portion of the control gate.

165. The method of claim 162, wherein the word line is formed on the first insulating layer such that the word line has a substantially planar upper surface.

166. The method of claim 162, wherein:

the step of exposing the top portion of the control gate comprises planarizing the first insulating layer to expose the control gate; and

wherein the step of forming a word line comprises depositing the word line over the first insulating layer, such that it contacts the exposed control gate.

167. The method of claim 162, wherein:

the step of providing the active area comprises forming a polysilicon active layer over an interlayer insulating layer;

the step of forming the charge storage region comprises forming an ONO dielectric film or an insulating layer containing conductive nanocrystals; and

the step of forming the word line comprises depositing at least one conductive layer over the first insulating layer and the exposed control gate, forming a first photoresist mask on the at least one conductive layer, and etching the at least one conductive layer to form the word line.

168. The method of claim 167, further comprising etching the active area and the charge storage region using the word line as a mask, such that the word line is self aligned to an EEPROM channel and the charge storage region.

169. The method of claim 168, further comprising:

forming sidewall spacers adjacent to the control gate sidewalls;

forming a metal layer over the control gate, the sidewall spacers and the doped source and drain regions;

heating the metal layer to form metal silicide regions over the source and drain regions; and

selectively removing the metal layer from the sidewall spacers.

170. The method of claim 169, wherein:

the doped source and drain regions and the silicide regions comprise bit lines which extend substantially perpendicular to a source-channel-drain direction; and

the word line extends substantially parallel to the source-channel-drain direction.

171. The method of claim 170, wherein the step of forming a polysilicon active layer comprises:

forming an amorphous silicon layer or a polysilicon layer;

heating the EEPROM after forming the metal layer to recrystallize the amorphous silicon layer or the polysilicon layer using the metal layer as a catalyst.

172. The method of claim 162, wherein the EEPROM is formed using two photolithographic masking steps.

173. A method of making an EEPROM, comprising:

providing a semiconductor active area;

forming a tunnel dielectric layer over the active area;

forming a conductive gate layer over the tunnel dielectric layer;

patterning the gate layer to form a floating gate overlying the tunnel dielectric layer;

doping the active area using the floating gate as a mask to form source and drain regions in the active area;

forming sidewall spacers adjacent to the floating gate sidewalls;

forming a first insulating layer above and adjacent to the sidewall spacers and above the source and drain regions;

forming a control gate dielectric layer over the floating gate; and

forming a word line over the control gate dielectric and over the first insulating layer.

174. The method of claim 173, further comprising:

forming a blocking layer above the gate layer, where the blocking layer comprises a different material than a material of the sidewall spacers and a material of the gate layer;

patterning the blocking layer during the step of patterning the gate layer;

forming the sidewall spacers such that they are located adjacent to the blocking layer sidewalls in addition to being formed adjacent to the floating gate sidewalls;

planarizing the first insulating layer to expose the blocking layer;

selectively removing the blocking layer from between the sidewall spacers to form a gate contact via;

forming the control gate dielectric in the gate contact via; and

forming a control gate in the gate contact via above the control gate dielectric by depositing a portion of the word line in the gate contact via.

175. The method of claim 173, further comprising:

planarizing the first insulating layer to expose a top portion of the floating gate;

forming the control gate dielectric over the first insulating layer, over the sidewall spacers and over the floating gate; and

forming the word line over the control gate dielectric such that the word line acts as a control gate of the EEPROM.

176. The method of claim 175, further comprising forming an upper portion of the floating gate which extends vertically and laterally above the sidewall spacers.

177. The method of claim 176, further comprising forming a hemispherical grain silicon upper portion of the floating gate.

178. The method of claim 177, further comprising roughening an upper surface of the upper portion of the floating gate.

179. The method of claim 173, further comprising:

forming a metal layer over the floating gate, the sidewall spacers and the doped source and drain regions;

heating the metal layer to form metal silicide regions over the source and drain regions; and

selectively removing the metal layer from the sidewall spacers.

180. The method of claim 179, wherein:

the doped source and drain regions and the silicide regions comprise bit lines which extend substantially perpendicular to a source-channel-drain direction; and

the word line extends substantially parallel to the source-channel-drain direction.

181. A method of forming a nonvolatile memory array, comprising:

forming a semiconductor active layer;

forming a first insulating layer over the active layer;

forming a plurality of gate electrodes over the first insulating layer;

doping the active layer using the gate electrodes as a mask to form a plurality of source and drain regions in the active layer, and a plurality of bit lines extending substantially perpendicular to a source-drain direction;

forming a second insulating layer above and adjacent to the gate electrodes and above the source regions, drain regions and the bit lines;

planarizing the second insulating layer; and

forming a plurality of word lines over the second insulating layer extending substantially parallel to the source-drain direction.

182. The method of claim 181, wherein each cell of the memory device comprising a gate electrode, a source, a drain, a channel, a portion of a word line and portions of two bit lines, is made using only two photolithographic masking steps.

183. The method of claim 182, further comprising:

forming sidewall spacers adjacent to the gate electrode sidewalls;

forming a metal layer over the gate electrodes, the sidewall spacers, the doped source and drain regions and the bit lines;

heating the metal layer to form metal silicide regions over the source and drain regions and the bit lines; and

selectively removing the metal layer from the sidewall spacers.

184. The method of claim 181, wherein the gate electrodes comprise EEPROM control gates and the insulating layer comprises an EEPROM charge storage region.

185. The method of claim 184, wherein the word lines are self aligned to the control gates.

186. The method of claim 181, wherein the gate electrodes comprise EEPROM floating gates and the insulating layer comprises a tunnel dielectric layer.

187. The method of claim 181, wherein the step of forming the word lines comprises depositing at least one conductive layer over the second insulating layer, forming a first photoresist mask on the at least one conductive layer, and etching the at least one conductive layer to form the word lines.

188. The method of claim 187, further comprising etching the active layer and the first insulating layer using the word line as a mask, such that the word line is self aligned to a plurality of EEPROM channels located in the active layer between the source and drain regions.

189. The method of claim 181, further comprising forming an interlayer insulating layer over the word lines and forming at least one additional device level of the array over the interlayer insulating layer.

190. The method of claim 189, further comprising:

forming a first via in the second insulating layer extending to a first word or bit line;

forming at least one conductive layer; and

patterning the conductive layer to form a plurality of word lines or word line contact layers and at least one bit line contact layer which contacts at least one of the plurality of the word or bit lines through the first via.

191. The method of claim 190, wherein:

the first via extends through the interlayer insulating layer in addition to extending through the second insulating layer; and

patterning the at least one conductive layer comprises forming a plurality of word line contact layers in an N+1st level of the array and forming at least one word or bit line contact layer in the Nth level of the array.

192. The method of claim 189, further comprising activating the doped source and drain regions in a plurality of device levels of the array during a same annealing step.

193. The method of claim 189, further comprising recrystallizing the active layers in a plurality of device levels of the array during a same annealing step.

194. The method of claim 193, further comprising activating the doped source and drain regions in the plurality of device levels of the array during the same annealing step as the recrystallizing step.

195. A method of making an EEPROM array, comprising:

providing a semiconductor active area;

forming a plurality of dummy blocks above the active area;

doping the active area using the dummy blocks as a mask to form source and drain regions in the active area;

forming an intergate insulating layer above and between the dummy blocks;

planarizing the intergate insulating layer to expose top portions of the dummy blocks;

selectively removing the dummy blocks from between portions of the planarized intergate insulating layer to form a plurality of vias between the portions of the intergate insulating layer;

forming charge storage regions over the active area in the plurality of vias;

forming a conductive gate layer over the charge storage regions; and

patterning the conductive gate layer to form a control gate overlying the charge storage region.

196. The method of claim 195, wherein the charge storage regions comprise an ONO dielectric film or an insulating layer containing conductive nanocrystals.

197. The method of claim 195, wherein the charge storage regions comprises a floating gate between a tunnel dielectric and a control gate dielectric.

198. The method of claim 195, wherein the dummy blocks comprise PECVD silicon nitride.

199. The method of claim 195, wherein the dummy blocks comprise a sacrificial conductive gate and a protective insulating layer.

200. The method of claim 199, further comprising forming sidewall spacers on sidewalls of the dummy blocks.

201. The method of claim 195, wherein:

the active area comprises an amorphous silicon or polysilicon layer formed over an interlayer insulating layer; and

the dummy block material is deposited at a temperature below 600 °C.

202. The method of claim 201, further comprising:

forming a metal layer over the dummy blocks and over exposed source and drain regions in the active area;

annealing the metal layer to form silicide regions over the source and drain regions; and

selectively removing unreacted portions of the metal layer remaining over the dummy blocks.

203. The method of claim 202, further comprising recrystallizing the active area using the silicide regions as a catalyst.

204. The method of claim 202, wherein the silicide regions comprise buried bit lines which extend in a direction substantially perpendicular to a source to drain direction.

205. The method of claim 204, wherein the step of patterning the conductive gate layer comprises forming a plurality of control gates in the vias above the charge storage regions and forming a plurality of word lines above the intergate insulating layer.

206. The method of claim 195, wherein each charge storage region contains a first horizontal portion above the active area in the via, vertical portions in the via adjacent to the intergate insulating layer sidewalls, and a second horizontal portion above the intergate insulating layer.

207. The method of claim 195, further comprising forming an interlayer insulating layer over the EEPROM array, and forming at least one more EEPROM array above the interlayer insulating layer.

208. A method of forming a TFT EEPROM, comprising:

forming a TFT EEPROM comprising an amorphous silicon or a polysilicon active layer, a charge storage region and a control gate;

providing a crystallization catalyst in contact with the active layer; and

heating the active layer after the step of providing the catalyst to recrystallize the active layer using the catalyst.

209. The method of claim 208, further comprising:

forming a plurality of crystallization windows above the active layer; and

providing the crystallization catalyst into the crystallization windows.

210. The method of claim 209, wherein the step of forming the plurality of crystallization windows comprises:

forming an insulating layer above the TFT EEPROM; and

patterning the insulating layer to simultaneously form crystallization window boundaries and sidewall spacers.

211. The method of claim 210, wherein the sidewall spacers are formed on a sacrificial gate.

212. The method of claim 211, further comprising:

removing the sacrificial gate; and

forming the charge storage region and the control gate after removing the sacrificial gate and after the step of heating.

213. The method of claim 208, wherein the catalyst comprises Ni, Ge, Mo, Co, Pt, Pd or a silicide thereof.

214. The method of claim 208, further comprising:

forming source and drain regions in the active layer;

forming a metal silicide crystallization catalyst in contact with the source and drain regions; and

recrystallizating the active layer using the metal silicide as the crystallization catalyst.

215. A method of forming a three dimensional array of TFT EEPROMs of claim 208, further comprising:

forming at least one interlayer insulating layer above the TFT EEPROM; and

forming a plurality of second TFT EEPROMs over the at least one interlayer insulating layer.

216. The method of claim 215, further comprising recrystallizing active layers in the TFTs in a plurality of device levels of the array during a same annealing step.

217. The method of claim 216, further comprising activating TFT doped source and drain regions in the plurality of device levels of the array during the same annealing step as the recrystallizing step.

218. An array of semiconductor devices disposed above a substrate, the array comprising:

a first plurality of spaced-apart conductors disposed at a first height above the substrate in a first direction; and

a second plurality of spaced-apart rail-stacks disposed at a second height in a second direction different from the first direction, each rail-stack including:

a semiconductor film whose first surface is in contact with said first plurality of spaced-apart conductors;

a conductive film; and

a local charge storage film disposed between a second surface of the semiconductor film and the conductive film.

219. The memory array of claim 218, wherein the second plurality of spaced-apart rail-stacks are disposed above the first plurality of spaced-apart conductors.

220. The memory array of claim 218 wherein a space between said spaced-apart conductors contains a planarized deposited oxide material.

221. The memory array of claim 218 wherein said semiconductor film comprises polysilicon.

222. The memory array of claim 221 wherein said polysilicon is P-doped.

223. The memory array of claim 222 wherein said P- doped polysilicon includes N+ outdiffusion regions at contacting intersections between said spaced-apart conductors and said spaced-apart rail-stacks.

224. The memory array of claim 218 wherein said local charge storage film comprises a charge trapping medium.

225. The memory array of claim 224 wherein said charge trapping medium comprises a dielectric isolated floating gate.

226. The memory array of claim 224 wherein said charge trapping medium comprises electrically isolated nanocrystals.

227. The memory array of claim 224 wherein said charge trapping medium comprises a charge trapping layer of a dielectric stack.

228. The memory array of claim 227 wherein said dielectric stack comprises an O-N-O dielectric stack.

229. The memory array of claim 224 wherein said conductive film comprises conductive polysilicon.

230. The memory array of claim 229 wherein said conductive film comprises a film including a conductive metal.

231. The memory array of claim 218 wherein said spaced-apart conductors comprise polysilicon.

232. The memory array of claim 231 wherein said spaced-apart conductors comprise a film including a conductive metal.

233. The memory array of claim 231 wherein said polysilicon of said spaced-apart conductors comprises polysilicon of a second conductivity type.

234. The memory array of claim 233 wherein said polysilicon of the second conductivity type is N+ doped.

235. The memory array of claim 218 wherein said semiconductor film comprises polysilicon.

236. The memory array of claim 235 wherein said first conductivity type is P- doped.

237. The memory array of claim 236 wherein said P- doped semiconductor film includes N+ outdiffusion regions at contacting intersections between said first plurality of spaced-apart conductors and said second plurality of spaced-apart rail stacks.

238. The memory array of claim 218, wherein:

the first plurality of spaced-apart conductors comprise doped polysilicon of a first conductivity type and an adjacent layer comprising a metal or a metal silicide; and

the conductive film comprises doped polysilicon of the first conductivity type and an adjacent layer comprising a metal or a metal silicide.

239. An array of semiconductor devices disposed above a substrate, the array comprising:

a first plurality of spaced-apart conductors disposed at a first height above the substrate in a first direction; and

a second plurality of spaced-apart rail-stacks disposed at a second height in a second direction different from the first direction, each rail-stack including:

a semiconductor film whose first surface is in contact with said first plurality of spaced-apart conductors;

a conductive film; and

a local charge storage film disposed between a second surface of the semiconductor film and the conductive film;

an isolation film;

a third plurality of spaced-apart conductors disposed at a third height above the isolation film in the first direction;

a fourth plurality of spaced-apart rail-stacks disposed at a fourth height above the isolation film in a second direction different from the first direction, each rail-stack including:

a semiconductor film whose first surface is in contact with said third plurality of spaced-apart conductors;

a conductive film; and

a local charge storage film disposed between a second surface of the semiconductor film and the conductive film.

240. The memory array of claim 239, wherein:

the second plurality of spaced-apart rail-stacks is disposed above a first plurality of spaced-apart conductors;

the isolation film is disposed above a second plurality of spaced-apart rail-stacks;

the third plurality of spaced-apart conductors is disposed above the isolation film;

the fourth plurality of spaced-apart rail-stacks is disposed above the third plurality of spaced-apart conductors.

241. The memory array of claim 239 wherein a space between said spaced-apart conductors contains a planarized deposited oxide material.

242. The memory array of claim 239 wherein said semiconductor films comprise P- doped polysilicon.

243. The memory array of claim 242 wherein said P- doped polysilicon includes N+ outdiffusion regions at contacting intersections between said spaced-apart conductors and said spaced-apart rail-stacks.

244. The memory array of claim 239 wherein said local charge storage films comprise a charge trapping medium.

245. The memory array of claim 244 wherein said charge trapping medium comprises a dielectric isolated floating gate.

246. The memory array of claim 244 wherein said charge trapping medium comprises electrically isolated nanocrystals.

247. The memory array of claim 244 wherein said charge trapping medium comprises a charge trapping layer of a dielectric stack.

248. The memory array of claim 247 wherein said dielectric stack comprises an O-N-O dielectric stack.

249. The memory array of claim 244 wherein said conductive films comprise conductive polysilicon.

250. The memory array of claim 249 wherein said conductive films comprise a film including a conductive metal.

251. The memory array of claim 239 wherein said spaced-apart conductors comprise polysilicon.

252. The memory array of claim 251 wherein said spaced-apart conductors comprise a film including a conductive metal.

253. The memory array of claim 251 wherein said polysilicon of said spaced-apart conductors comprises polysilicon of a second conductivity type.

254. The memory array of claim 253 wherein said polysilicon of the second conductivity type is N+ doped.

255. The memory array of claim 239 wherein said semiconductor films comprise polysilicon.

256. The memory array of claim 255 wherein said semiconductor film polysilicon is P- doped.

257. The memory array of claim 256 wherein said P- doped semiconductor films include N+ outdiffusion regions at contacting intersections between said first plurality of spaced-apart conductors and said second plurality of spaced-apart rail stacks.

258. The memory array of claim 239, wherein:

the first and the third plurality of spaced-apart conductors comprise doped polysilicon of a first conductivity type and an adjacent layer comprising a metal or a metal silicide; and

the conductive film comprises doped polysilicon of the first conductivity type and an adjacent layer comprising a metal or a metal silicide.

259. A memory array disposed above a substrate, the array comprising:

a first plurality of first spaced-apart rail-stacks disposed at a first height above the substrate in a first direction, each first rail-stack including:

a conductive film;

a local charge storage film disposed above the conductive film; and

a semiconductor film disposed above the local charge storage film;

a second plurality of spaced-apart conductors disposed at a second height above said first height in a second direction different from the first direction; and

a third plurality of second spaced-apart rail-stacks disposed at a third height above the second height in the first direction, each second rail-stack including:

a semiconductor film;

a local charge storage film disposed above the semiconductor film; and

a conductive film disposed above the local charge storage film.

260. The memory array of claim 259, wherein the second plurality of spaced-apart conductors contact the semiconductor films in the first and the third rail stacks.

261. The memory array of claim 260, wherein the second plurality of spaced-apart conductors contact doped source or drain regions in the semiconductor films in the first and the third rail stacks.

262. A memory array disposed above a substrate, the array comprising:

a first plurality of spaced-apart rail-stacks disposed at a first height above the substrate in a first direction, each rail-stack including a conductive film, a local charge storage film disposed above the conductive film and a semiconductor film disposed above the local charge storage film; and

a first plurality of spaced-apart conductors disposed at a second height above the first height in a second direction different from the first direction, said spaced-apart conductors overlying regions of the semiconductor film that contain impurities, the regions forming an electrical connection between the spaced-apart conductors and the local charge storage film.

263. The memory array of claim 262, further comprising:

a third plurality of spaced-apart rail-stacks disposed at a third height above the second height in the first direction, each rail-stack including a conductive film, a local charge storage film disposed above the conductive film, and a second semiconductor film disposed above the local charge storage film; and

a fourth plurality of spaced-apart conductors disposed at a fourth height above the third height in the second direction, said spaced-apart conductors overlying regions of the second semiconductor film that contain impurities, the regions forming an electrical connection between the spaced-apart conductors and the local charge storage film.

264. The memory array of claim 262 wherein a space between said spaced-apart conductors contains a planarized oxide material

265. A memory array disposed above a substrate, the array comprising:

a first plurality of spaced-apart rail-stacks disposed at a first height above the substrate in a first direction, each rail-stack including a conductive film and a local charge storage film disposed above the conductive film;

a first plurality of spaced-apart conductors disposed at a second height above the first height in a second direction different from the first direction, said spaced-apart conductors making contacting intersections with said rail stacks so that said spaced-apart conductors directly contact said local charge storage films at said contacting intersections; and

a semiconductor film disposed between said spaced-apart conductors and above said local charge storage films in a region about said contacting intersections.

266. The memory array of claim 265 wherein a space between said spaced-apart conductors contains a planarized oxide material

267. The memory array of claim 265 wherein said semiconductor film comprises polysilicon.

268. The memory array of claim 267 wherein said polysilicon semiconductor film is P- doped.

269. The memory array of claim 268 wherein said P- doped polysilicon includes N+ outdiffusion regions adjacent said spaced-apart conductors.

270. The memory array of claim 265 wherein said local charge storage film comprises a charge trapping medium.

271. The memory array of claim 270 wherein said charge trapping medium comprises a dielectric isolated floating gate.

272. The memory array of claim 270 wherein said charge trapping medium comprises electrically isolated nanocrystals.

273. The memory array of claim 270 wherein said charge trapping medium comprises a charge trapping layer of a dielectric stack.

274. The memory array of claim 273 wherein said dielectric stack comprises an O-N-O dielectric stack.

275. The memory array of claim 270 wherein said conductive film comprises conductive polysilicon.

276. The memory array of claim 275 wherein said conductive film comprises a film including a conductive metal.

277. The memory array of claim 265 wherein said spaced-apart conductors comprise polysilicon.

278. The memory array of claim 277 wherein said spaced-apart conductors comprise a film including a conductive metal.

279. The memory array of claim 277 wherein said polysilicon of said spaced-apart conductors comprises polysilicon of a second conductivity type.

280. The memory array of claim 277 wherein said polysilicon of the second conductivity type is N+ doped.

281. The memory array of claim 265 wherein said semiconductor film comprises polysilicon.

282. The memory array of claim 281 wherein said semiconductor film polysilicon is P- doped.

283. The memory array of claim 282 wherein said P- doped semiconductor film includes N+ outdiffusion regions at contacting intersections between said first plurality of spaced-apart conductors and said second plurality of spaced-apart rail stacks.

284. The memory array of claim 265, wherein:

the first plurality of spaced-apart conductors comprise doped polysilicon of a first conductivity type and an adjacent layer comprising a metal or a metal silicide;

the conductive film comprises doped polysilicon of the first conductivity type and an adjacent layer comprising a metal or a metal silicide.

285. The memory array of claim 265, wherein the array comprises a monolithic three dimensional array.

286. A method for programming a memory cell of a three-dimensional array of NMOS memory cells with two bits of information, the array of memory cells disposed above a substrate and including a first plurality, Z, of memory levels, the z-th memory level including a second plurality, X, of bit line conductors and a third plurality, Y, of word line conductors, the memory cells having a local charge storage medium, said method comprising:

providing a first potential, a second potential and a third potential, said first potential being less than said second potential and said second potential being less than said third potential;

selecting for programming a memory cell at a location defined by wordline y, level z and disposed between bitlines x and x+1;

programming the first of the two bits by:

applying said first potential to all bitlines less than or equal to x on the z-th level;

applying said second potential to all bitlines greater than x on the z-th level;

applying said third potential to wordline y on the z-th level; and

applying said first potential to all wordlines other than y on the z-th level and to all wordlines and bitlines on levels other than the z-th level; and

programming the second of the two bits by:

applying said first potential to all bitlines greater than x on the z-th level;

applying said second potential to all bitlines less than or equal to x on the z-th level;

applying said third potential to wordline y on the z-th level; and

applying said first potential to all wordlines other than y on the z-th level and to all wordlines and bitlines on levels other than the z-th level.

287. A method of claim 286 wherein said second potential is in a range of about 3 to about 8 volts greater than said first potential.

288. A method of claim 287 wherein said third potential is in a range of about 9 to about 13 volts greater than said first potential.

289. A method for programming a memory cell of a three-dimensional array of PMOS memory cells with two bits of information, the array of memory cells disposed above a substrate and including a first plurality, Z, of memory levels, the z-th memory level including a second plurality, X, of bit line conductors and a third plurality, Y, of word line conductors, the memory cells having a local charge storage medium, said method comprising:

providing a first potential, a second potential and a third potential, said first potential being greater than said second potential and said second potential being greater than said third potential;

selecting for programming a memory cell at a location defined by wordline y, level z and disposed between bitlines x and x+1;

programming the first of the two bits by:

applying said first potential to all bitlines less than or equal to x on the z-th level;

applying said second potential to all bitlines greater than x on the z-th level;

applying said third potential to wordline y on the z-th level; and

applying said first potential to all wordlines other than y on the z-th level and to all wordlines and bitlines on levels other than the z-th level; and

programming the second of the two bits by:

applying said first potential to all bitlines greater than x on the z-th level;

applying said second potential to all bitlines less than or equal to x on the z-th level;

applying said third potential to wordline y on the z-th level; and

applying said first potential to all wordlines other than y on the z-th level and to all wordlines and bitlines on levels other than the z-th level.

290. A method of claim 289 wherein said second potential is in a range of about 3 to about 8 volts less than said first potential.

291. A method of claim 290 wherein said third potential is in a range of about 9 to about 13 volts less than said first potential.

292. A method for reading the contents of a memory cell of a three-dimensional array of NMOS memory cells with two bits of information stored in the memory cell, the array of memory cells disposed above a substrate and including a first plurality, Z, of memory levels, the z-th memory level including a second plurality, X, of bit line conductors and a third plurality, Y, of word

line conductors, the memory cells having a local charge storage medium, said method comprising:

providing a first potential, a second potential and a third potential, said first potential being less than said second potential and said second potential being less than said third potential;

selecting for reading a memory cell at a location defined by wordline y, level z and disposed between bitlines x and x+1;

applying said second potential to all bitlines less than or equal to x on the z-th level;

applying said first potential to all bitlines greater than x on the z-th level;

applying said third potential to wordline y on the z-th level; and

applying said first potential to all wordlines other than y on the z-th level and to all wordlines and bitlines on levels other than the z-th level; and

applying said second potential to all bitlines greater than x on the z-th level;

applying said first potential to all bitlines less than or equal to x on the z-th level;

applying said third potential to wordline y on the z-th level; and

applying said first potential to all wordlines other than y on the z-th level and to all wordlines and bitlines on levels other than the z-th level.

293. A method of claim 292 wherein said second potential is in a range of about 50 milivolts to about 3 volts greater than said first potential.

294. A method of claim 293 wherein said third potential is in a range of about 1 to about 5 volts greater than said first potential.

295. A method for reading the contents of a memory cell of a three-dimensional array of PMOS memory cells with two bits of information stored in the memory cell, the array of memory cells disposed above a substrate and including a first plurality, Z, of memory levels, the z-th memory level including a second plurality, X, of bit line conductors and a third plurality, Y, of word line conductors, the memory cells having a local charge storage medium, said method comprising:

providing a first potential, a second potential and a third potential, said first potential being greater than said second potential and said second potential being greater than said third potential;

selecting for reading a memory cell at a location defined by wordline y, level z and disposed between bitlines x and x+1;

applying said second potential to all bitlines less than or equal to x on the z-th level;

applying said first potential to all bitlines greater than x on the z-th level;

applying said third potential to wordline y on the z-th level; and

applying said first potential to all wordlines other than y on the z-th level and to all wordlines and bitlines on levels other than the z-th level; and

applying said second potential to all bitlines greater than x on the z-th level;

applying said first potential to all bitlines less than or equal to x on the z-th level;

applying said third potential to wordline y on the z-th level; and

applying said first potential to all wordlines other than y on the z-th level and to all wordlines and bitlines on levels other than the z-th level.

296. A method of claim 295 wherein said second potential is in a range of about 50 milivolts to about 3 volts less than said first potential.

297. A method of claim 296 wherein said third potential is in a range of about 1 to about 5 volts less than said first potential.

298. A method for erasing the contents of all memory cells belonging to a three-dimensional array of NMOS memory cells with two bits of information stored per memory cell, the array of memory cells disposed above a substrate and including a first plurality, Z, of memory levels, the z-th memory level including a second plurality, X, of bit line conductors and a third plurality, Y, of word line conductors, the memory cells having a local charge storage medium, said method comprising:

providing a first potential and a second potential, said first potential being less than said second potential;

applying said second potential to all bitlines; and

applying said first potential to all wordlines.

299. A method of claim 298 wherein said second potential is in a range of about 5 to about 15 volts greater than said first potential.

300. A method for erasing the contents of all memory cells of a three-dimensional array of PMOS memory cells with two bits of information stored per memory cell, the array of memory cells disposed above a substrate and including a first plurality, Z, of memory levels, the z-th memory level including a second plurality, X, of bit line conductors and a third plurality, Y,

of word line conductors, the memory cells having a local charge storage medium, said method comprising:

providing a first potential and a second potential, said first potential being greater than said second potential;

applying said second potential to all bitlines; and

applying said first potential to all wordlines.

301. A method of claim 300 wherein said second potential is in a range of about 5 to about 15 volts less than said first potential.

302. A method for erasing a single bit of a memory cell of a three-dimensional array of NMOS memory cells with two bits of information, the array of memory cells disposed above a substrate and including a first plurality, Z, of memory levels, the z-th memory level including a second plurality, X, of bit line conductors and a third plurality, Y, of word line conductors, the memory cells having a local charge storage medium, said method comprising:

providing a first potential, a second potential and a third potential, said first potential being less than or equal to said second potential and said second potential being less than said third potential;

selecting for erasure a memory storage location of a memory cell at a location defined by wordline y, level z and disposed between bitlines x and x+1, the storage location being adjacent bitline x+1;

reading the contents of a memory storage location of a memory cell at a location defined by wordline y, level z and disposed between bitlines x+1 and x+2, the storage location being adjacent bitline x+1;

storing said contents in a memory store;

applying said first potential to wordline y;

applying said second potential to all bitlines other than bitline x+1;

applying said third potential to bitline x+1;

floating all wordlines other than wordline y;

applying said first potential to or floating all bitlines and wordlines on levels other than the z-th level;

retrieving said contents from said memory store; and

writing said contents to said memory storage location of the memory cell at the location defined by wordline y, level z and disposed between bitlines x+1 and x+2, the storage location being adjacent bitline x+1.

303. A method of claim 302 wherein said second potential is in a range of about 0 to about 5 volts greater than said first potential.

304. A method of claim 303 wherein said third potential is in a range of about 5 to about 15 volts greater than said first potential.

305. A method for erasing a single bit of a memory cell of a three-dimensional array of PMOS memory cells with two bits of information, the array of memory cells disposed above a substrate and including a first plurality, Z, of memory levels, the z-th memory level including a second plurality, X, of bit line conductors and a third plurality, Y, of word line conductors, the memory cells having a local charge storage medium, said method comprising:

providing a first potential, a second potential and a third potential, said first potential being greater than or equal to said second potential and said second potential being greater than said third potential;

selecting for erasure a memory storage location of a memory cell at a location defined by wordline y, level z and disposed between bitlines x and x+1, the storage location being adjacent bitline x+1;

reading the contents of a memory storage location of a memory cell at a location defined by wordline y, level z and disposed between bitlines x+1 and x+2, the storage location being adjacent bitline x+1;

storing said contents in a memory store;

applying said first potential to wordline y;

applying said second potential to or floating all bitlines other than bitline x+1;

applying said third potential to bitline x+1;

floating all wordlines other than wordline y;

applying said first potential to all bitlines and wordlines on levels other than the z-th level;

retrieving said contents from said memory store; and

writing said contents to said memory storage location of the memory cell at the location defined by wordline y, level z and disposed between bitlines x+1 and x+2, the storage location being adjacent bitline x+1.

306. A method in accordance with claim 305 wherein said second potential is in a range of about 0 to about 5 volts less than said first potential.

307. A method in accordance with claim 306 wherein said third potential is in a range of about 5 to about 15 volts less than said first potential.

308. A method for manufacturing a three-dimensional array of TFT memory cells, said method comprising:

(a) disposing an isolation layer over a substrate;

(b) disposing a first plurality of spaced-apart conductors in a first direction over the isolation layer;

(c) disposing an insulating layer over said first plurality of spaced-apart conductors and thereby filling a space between said spaced-apart conductors with the insulating material;

(d) planarizing the insulating layer to expose the first plurality of spaced-apart conductors;

(e) disposing a second plurality of rail stacks in a second direction over and in contact with said first plurality of spaced-apart conductors, said rail stacks including a first layer of a semiconductor material of a first conductivity type, a second layer including a local charge storage film, and a third conductive layer.

309. The method of claim 308, further comprising:

(f) repeating (a), (b), (c), (d) and (e) a desired number of times to form a desired number of levels of TFT memory cells.

310. The method of claim 308, wherein the step of planarizing comprises CMP.

311. The method of claim 310, further comprising CMP planarizing the isolation layer.

312. The method of claim 308, further comprising:

(g) outdiffusing source and drain dopants from the first plurality of spaced-apart second conductivity type doped polysilicon conductors into the first layer of a semiconductor material.

313. The method of claim 312, further comprising repeating (a), (b), (c), (d), (e), (f) and (g) a desired number of times to form a desired number of levels of TFT memory cells.

314. A method for manufacturing a three-dimensional array of TFT memory cells, said method comprising:

(a) disposing an isolation layer over a substrate;

(b) disposing a first plurality of spaced-apart conductors in a first direction over the isolation layer;

(c) disposing rails of local charge storage film in the first direction over and in contact with said first plurality of spaced-apart conductors;

(d) disposing a second plurality of spaced-apart conductors in a second direction over and in contact with the local charge storage film, the conductors formed of a polysilicon material of a first conductivity type;

(e) disposing a semiconductor film of a second conductivity type in between ones of said second plurality of spaced-apart conductors;

(f) disposing an insulating layer over said semiconductor film and said second plurality of spaced-apart conductors and thereby filling a

space between said second spaced-apart conductors with the insulating material; and

(g) planarizing the insulating layer.

315. The method of claim 314, further comprising:

(h) repeating (a), (b), (c), (d), (e), (f) and (g) a desired number of times to form a desired number of levels of TFT memory cells.

316. A method for manufacturing a three-dimensional array of TFT memory cells, said method comprising:

(a) disposing an isolation layer over a substrate;

(b) disposing a first plurality of spaced-apart conductors in a first direction over the isolation layer;

(c) disposing a first local charge storage film over the first plurality of spaced-apart conductors;

(d) disposing a first layer of a semiconductor material of a first conductivity type over said local charge storage film;

(e) disposing a second plurality of spaced-apart conductors formed of a doped semiconductor material of a second conductivity type in a second direction over the first layer of semiconductor material;

(f) disposing an insulating layer over said second plurality of spaced-apart conductors and thereby filling a space between said second spaced-apart conductors with the insulating material;

(g) planarizing to expose said second spaced-apart conductors;

(h) disposing a second layer of a semiconductor material of a first conductivity type over said second spaced-apart conductors;

(i) disposing a second local charge storage film over the second layer of semiconductor material;

(j) disposing a first plurality of spaced-apart conductors in the first direction over the second local charge storage film; and

(k) forming outdiffusion regions in said first and second layers of semiconductor material of the first conductivity type at intersections between said layers and said spaced-apart conductors.

317. The method of claim 316, further comprising:

(l) repeating (c), (d), (e), (f), (g), (h), (i), (j) and (k) a desired number of times to form a desired number of levels of TFT memory cells.

318. A method for manufacturing an array of TFT memory cells, said method comprising:

disposing an isolation layer over a substrate;

disposing a first plurality of rail-stacks in a first direction over the isolation layer, said rail-stacks including a conductive film layer, a local charge storage film layer disposed over said conductive film layer, and a semiconductor film layer of a first conductivity type disposed over said local charge storage film layer;

disposing an oxide layer over said rail-stacks;

masking the oxide layer;

etching the oxide layer;

removing the mask;

implanting impurities of the second conductivity type through apertures etched in the oxide layer and into the semiconductor film layer;

depositing a conductive film into said aperture; and

planarizing the conductive layer.

319. A method for manufacturing an array of TFT memory cells, said method comprising:

disposing an isolation layer over a substrate;

disposing a layer of amorphous silicon of a first conductivity type over said isolation layer;

disposing a silicon nitride CMP stop layer over said amorphous silicon layer;

masking the silicon nitride layer;

etching apertures defined by the masking into said isolation layer;

depositing a conductive layer of a semiconductor material of the second conductivity type into and over the apertures;

planarizing said conductive layer to said CMP stop layer;

disposing a local charge storage film over said CMP stop layer; and

disposing a conductive film over said charge storage film.

320. A memory array disposed above a substrate, the array comprising:

an insulator layer;

a first plurality of spaced-apart conductors disposed in the insulator layer in a first direction;

semiconductor regions of a first conductivity type disposed between and in contact with adjacent areas of said spaced-apart conductors; and

a second plurality of spaced-apart rail-stacks disposed in a second direction above and in contact with the first plurality of spaced-apart

conductors, each rail-stack including a local charge storage film and a conductive film disposed above the local charge storage film.

321. The memory array of claim 320 wherein said semiconductor film comprises polysilicon.

322. The memory array of claim 321 wherein said polysilicon is P-doped.

323. The memory array of claim 322 wherein said P- doped polysilicon includes N+ outdiffusion regions at contacts between said spaced-apart conductors and said semiconductor regions.

324. The memory array of claim 320 wherein said local charge storage film comprises a charge trapping medium.

325. The memory array of claim 324 wherein said charge trapping medium comprises a dielectric isolated floating gate.

326. The memory array of claim 324 wherein said charge trapping medium comprises electrically isolated nanocrystals.

327. The memory array of claim 324 wherein said charge trapping medium comprises a charge trapping layer of a dielectric stack.

328. The memory array of claim 327 wherein said dielectric stack comprises an O-N-O dielectric stack.

329. The memory array of claim 324 wherein said conductive film comprises conductive polysilicon.

330. The memory array of claim 329 wherein said conductive film comprises a film including a conductive metal.

331. The memory array of claim 320 wherein said spaced-apart conductors comprise polysilicon.

332. The memory array of claim 331 wherein said spaced-apart conductors comprise a film including a conductive metal.

333. The memory array of claim 331 wherein said polysilicon of said spaced-apart conductors comprises polysilicon of a second conductivity type.

334. The memory array of claim 333 wherein said polysilicon of the second conductivity type is N+ doped.

335. The memory array of claim 320 wherein said semiconductor film comprises polysilicon.

336. The memory array of claim 335 wherein said first conductivity type is P-.

337. The memory array of claim 320, further comprising:

an isolation film disposed over said second plurality of spaced-apart rail-stacks;

a third plurality of spaced-apart conductors disposed in the isolation film in the first direction;

a plurality of semiconductor regions of the first conductivity type disposed between and in contact with adjacent ones of said spaced-apart conductors; and

a fourth plurality of spaced-apart rail-stacks disposed in the second direction above and in contact with the third plurality of spaced-apart conductors, each rail-stack including a local charge storage film and a conductive film disposed above the local charge storage film.

338. A TFT CMOS, comprising:

a gate electrode;

a first insulating layer adjacent to a first side of the gate electrode;

a first semiconductor layer having a first conductivity type disposed on a side of the first insulating layer opposite to the gate electrode;

first source and drain regions of a second conductivity type disposed in the first semiconductor layer;

first source and drain electrodes in contact with the first source and drain regions and disposed on a side of the first semiconductor layer opposite to the first insulating layer;

a second insulating layer adjacent to a second side of the gate electrode;

a second semiconductor layer having a second conductivity type disposed on a side of the second insulating layer opposite to the gate electrode;

second source and drain regions of a first conductivity type disposed in the second semiconductor layer; and

second source and drain electrodes in contact with the second source and drain regions and disposed on a side of the second semiconductor layer opposite to the second insulating layer.

339. The TFT CMOS of claim 338, further comprising:

a semiconductor substrate;

an interlayer insulating layer between the substrate and the TFT CMOS;

a first planar insulating filler layer disposed between the first source and drain electrodes; and

a first planar insulating filler layer disposed between the second source and drain electrodes.

340. The TFT CMOS of claim 339, wherein:

the first source and drain electrodes comprise second conductivity type polysilicon rails which extend above the interlayer insulating layer in a first plane;

the first semiconductor layer comprises a polysilicon layer which extends above the first source and drain electrodes in a second plane;

the gate electrode comprises a first polysilicon layer of a second conductivity type, a silicide layer over the first polysilicon layer and a second polysilicon layer of a first conductivity type above the silicide layer, wherein the gate electrode extends above the first insulating layer in a third plane;

the second semiconductor layer comprises a polysilicon layer which extends above the gate electrode in a fourth plane;

the second source and drain electrodes comprise first conductivity type polysilicon rails which extend above the second semiconductor layer in a fifth plane; and

wherein the first through the fifth planes do not overlap.

341. The TFT CMOS of claim 340, wherein:

the gate electrode, the first insulating layer, the first semiconductor layer, the second insulating layer and the second semiconductor layer comprise a rail stack which extends perpendicular to the first and to the second source and drain electrodes in a plane parallel to the substrate; and

the gate electrode, the first insulating layer, the first semiconductor layer, the second insulating layer and the second semiconductor layer are aligned in a plane perpendicular to the substrate and parallel to a source to drain direction.

342. The TFT CMOS of claim 340, further comprising:

a first charge storage region which includes the first insulating layer; and

a second charge storage region which includes the second insulating layer.

343. The TFT CMOS of claim 342, wherein:

the first charge storage region comprises an O-N-O stack, isolated nanocrystals or a floating gate between the first insulating layer and a control gate dielectric; and

the second charge storage region comprises an O-N-O stack, isolated nanocrystals or a floating gate between the first insulating layer and a control gate dielectric.

344. The TFT CMOS of claim 340, wherein the first insulating layer comprises a portion of a charge storage region while the second insulating layer does not comprise a portion of a charge storage region.

345. A monolithic three dimensional array comprising a plurality of device levels vertically separated by one or more interlayer insulating layers, wherein each device level contains a plurality of TFT CMOS devices of claim 344.

346. An array of semiconductor devices disposed above a substrate, the array comprising:

a first plurality of spaced-apart conductors disposed at a first height above the substrate in a first direction;

a second plurality of spaced-apart rail-stacks disposed at a second height above the first height in a second direction different from the first direction, each rail-stack including:

a first semiconductor film of a first conductivity type containing

a plurality of source and drain regions of a second conductivity type in contact with said first plurality of spaced-apart conductors;

a first local charge storage film disposed above the first semiconductor film;

a gate line disposed above the first local charge storage film;

a second local charge storage film disposed above the gate line;

a second semiconductor film of a second conductivity type containing a plurality of source and drain regions of a first conductivity type; and

a third plurality of spaced-apart conductors contacting the source and drain regions of a first conductivity type, wherein the third

plurality of spaced-apart conductors are disposed at a third height above the second plurality of spaced-apart rail-stacks.

347. The array of claim 346, wherein a space between said spaced-apart conductors contains a planar deposited insulating layer.

348. The array of claim 347 wherein said first and second semiconductor films comprise polysilicon layers.

349. The array of claim 348, wherein said first and second charge storage films comprise a charge trapping medium.

350. The array of claim 349, wherein said charge trapping medium comprises a dielectric isolated floating gate, electrically isolated nanocrystals, or O-N-O dielectric stack.

351. The array of claim 350, wherein the gate line comprises a first polysilicon layer of a second conductivity type adjacent to the first charge storage film, a silicide layer over the first polysilicon layer and a second polysilicon layer of a first conductivity type above the silicide layer adjacent to the second charge storage film.

352. The array of claim 351, wherein:

said first plurality of spaced-apart conductors comprise polysilicon layers of a second conductivity type; and

said third plurality of spaced-apart conductors comprise polysilicon layers of a first conductivity type.

353. The array of claim 352, wherein said plurality of first and third spaced-apart conductors further comprise a metal or silicide layer.

354. The array of claim 353, wherein the source and drain regions of a second conductivity type comprise outdiffusion regions.

355. The array of claim 346, wherein a TFT EEPROM CMOS device is formed at each intersection of the first and the third spaced-apart conductors and the gate line.

356. A monolithic three dimensional array comprising a plurality of device levels vertically separated by one or more interlayer insulating layers, wherein each device level contains the array of claim 346.

357. The array of claim 356, wherein the array comprises three or more device levels.

358. The array of claim 357, further comprising a driver circuit arranged in the substrate below the array and at least in partial vertical alignment with the array.

359. The array of claim 358, wherein:

the charge storage film comprises at least one insulating layer capable of storing charge; and

the driver circuit is adapted to provide a sufficient voltage between a spaced apart conductor and a gate line in a same device level to form a conductive link between the conductor and the gate line.

360. The array of claim 359, wherein at least one conductive link is formed between at least one conductor and at least one gate line.

361. The array of claim 360, wherein the array comprises at least one logic circuit.

362. The array of claim 361, wherein the at least one logic circuit comprises an inverter or a NAND gate.

363. The array of claim 360, wherein the array comprises a static random access memory.

364. A circuit comprising a plurality of charge storage devices and a plurality of antifuse devices.

365. The circuit of claim 364, wherein the plurality of charge storage devices and the plurality of antifuse devices comprise a same set of devices which function as charge storage devices when a first programming voltage is applied to the devices and which function as antifuses when a second programming voltage higher than a first voltage is applied to the devices, which is sufficient to form a conductive link through a charge storage region.

366. The circuit of claim 365, wherein the antifuse devices comprise devices in which a conductive link has been formed though the charge storage region of the charge storage device.

367. The circuit of claim 365, wherein the charge storage devices comprise semiconductor diodes containing a charge storage region.

368. The circuit of claim 367, wherein:

the diodes comprise polysilicon or amorphous silicon diodes arranged in a three dimensional monolithic array containing at least three device levels separated by interlayer insulating layers, the array being disposed above a substrate; and

the charge storage region comprises a stack of insulating layers located between p-doped and n-doped regions of the diodes or adjacent to the p-doped or n-doped regions of the diodes.

369. The circuit of claim 365, wherein the charge storage devices comprise EEPROM transistors.

370. The circuit of claim 369, wherein:

the transistors comprise polysilicon or amorphous silicon thin film transistors arranged in a three dimensional monolithic array containing at least three device levels separated by interlayer insulating layers, the array being disposed above a substrate; and

the charge storage region comprises a stack of insulating layers located between a channel and a control gate of the thin film transistors.

371. The circuit of claim 370, wherein at least one device level of the three dimensional monolithic array comprises:

a first plurality of spaced-apart conductors disposed at a first height above the substrate in a first direction; and

a second plurality of spaced-apart rail-stacks disposed at a second height in a second direction different from the first direction, each rail-stack including a semiconductor film in contact with said first plurality of

spaced-apart conductors, a local charge storage film disposed above the semiconductor film and a conductive film disposed above the local charge storage film.

372. The circuit of claim 365, further comprising a driver circuit which is adapted to provide the first programming voltage to a first set of charge storage devices to turn the first set of charge storage devices off by increasing a threshold voltage of the first set of charge storage devices and to provide the second programming voltage to a second set of charge storage devices to form a conductive link through the charge storage region of the second set of charge storage devices to convert the second set of charge storage devices to antifuse devices.

373. The circuit of claim 372, wherein the circuit comprises a field programmable gate array or a programmable logic device.

374. The circuit of claim 373, wherein the circuit is programmed to function as an inverter, a NAND gate or an SRAM.

375. The circuit of claim 373, wherein an area per logic gate in the circuit is $4(F(x+1))^2$ to $5(F(x+1))^2$, where F is the minimum feature size and x is the number of inputs on the logic gate.

376. A method of programming a circuit, comprising:

providing a circuit comprising a plurality of charge storage devices;

applying a first programming voltage to a first set of charge storage devices to turn the first set of charge storage devices off by increasing a threshold voltage of the first set of charge storage devices; and

applying a second programming voltage to a second set of charge storage devices to form a conductive link through a charge storage region of the second set of charge storage devices to convert the second set of charge storage devices to antifuse devices.

377. The method of claim 376, wherein the first and the second sets of charge storage devices comprise the same charge storage devices.

378. The method of claim 377, wherein the charge storage devices comprise semiconductor diodes containing a charge storage region.

379. The method of claim 378, wherein:

the diodes comprise polysilicon or amorphous silicon diodes arranged in a three dimensional monolithic array containing at least three device levels separated by interlayer insulating layers, the array being disposed above a substrate; and

the charge storage region comprises a stack of insulating layers located between p-doped and n-doped regions of the diodes or adjacent to the p-doped and n-doped regions of the diodes.

380. The method of claim 379, wherein the charge storage devices comprise EEPROM transistors.

381. The method of claim 380, wherein:

the transistors comprise polysilicon or amorphous silicon thin film transistors arranged in a three dimensional monolithic array containing at least three device levels separated by interlayer insulating layers, the array being disposed above a substrate; and

the charge storage region comprises a stack of insulating layers located between a channel and a control gate of the thin film transistors.

382. The method of claim 376, wherein the circuit is programmed to function as a logic gate.

383. The method of claim 376, wherein the circuit is programmed to function as a static random access memory.

384. A semiconductor device comprising:

a semiconductor active region;

a charge storage region adjacent to the semiconductor active region;

a first electrode; and

a second electrode;

wherein charge is stored in the charge storage region when a first programming voltage is applied between the first and the second electrodes, and a conductive link is formed through the charge storage region to form a conductive path between the first and the second electrodes when a second programming voltage higher than the first voltage is applied between the first and the second electrodes.

385. The device of claim 384, wherein the first programming voltage turns the device off by increasing a threshold voltage of the device.

386. The device of claim 384, wherein the device comprises a semiconductor diode containing the charge storage region.

387. The device of claim 386, wherein:

the diode comprises a polysilicon or an amorphous silicon diode arranged in a three dimensional monolithic array containing at least three device levels separated by interlayer insulating layers, the array being disposed above a substrate; and

the charge storage region comprises a stack of insulating layers located between p-doped and n-doped portions of the semiconductor active region of the diode or adjacent to the p-doped or n-doped portions of the semiconductor active region of the diode.

388. The device of claim 385, wherein the device comprises an EEPROM transistor.

389. The device of claim 388, wherein:

the semiconductor active region of the transistor comprises a polysilicon or an amorphous silicon thin film disposed on an insulating layer;

the transistor is arranged in a three dimensional monolithic array containing at least three device levels separated by interlayer insulating layers, the array being disposed above a substrate; and

the charge storage region comprises a stack of insulating layers located between a channel in the semiconductor active region and a control gate of the transistor.

390. The device of claim 384, wherein the device is arranged in a field programmable gate array or in a programmable logic device.

391. A method of making an array of semiconductor devices disposed above a substrate, comprising:

forming a first plurality of spaced-apart conductors disposed at a first height above the substrate in a first direction;

forming a first insulating layer over and between the first conductors;

planarizing the insulating layer to expose the first conductors;

forming a stack of layers comprising a first semiconductor layer of a first conductivity type in contact with said first plurality of spaced-apart conductors, a first local charge storage film disposed above the first semiconductor layer, a gate line disposed above the first local charge storage film, a second local charge storage film disposed above the gate line and a second semiconductor layer of a second conductivity type above the second local charge storage film;

patterning the stack of layers to form a second plurality of spaced-apart rail-stacks disposed at a second height above the first height in a second direction different from the first direction;

forming a second insulating layer above and between the rail stacks;

planarizing the second insulating layer;

forming a plurality of trenches in the second insulating layer;

forming a conductive layer in the trenches and over the second insulating layer; and

planarizing the conductive layer to form a third plurality of spaced-apart conductors disposed at a third height above the second plurality of spaced-apart rail-stacks.

392. The method of claim 391 wherein said first and second semiconductor layers comprise polysilicon layers.

393. The method of claim 392, wherein said first and second charge storage films comprise a charge trapping medium.

394. The method of claim 393, wherein said charge trapping medium comprises a dielectric isolated floating gate, electrically isolated nanocrystals, or O-N-O dielectric stack.

395. The method of claim 395, wherein the gate line comprises a first polysilicon layer of a second conductivity type adjacent to the first charge storage film, a silicide layer over the first polysilicon layer and a second polysilicon layer of a first conductivity type above the silicide layer adjacent to the second charge storage film.

396. The method of claim 391, further comprising outdiffusing dopants of a second conductivity type from the first conductors into the first semiconductor layer to form source and drain regions.

397. The method of claim 391, further comprising implanting ions of a first conductivity type into the trenches to form source and drain regions in the second semiconductor layer.

398. The method of claim 391, further comprising forming sidewall spacers on rail stack sidewalls prior to forming the second insulating layer.

399. The method of claim 391, wherein the second plurality of rail stacks are disposed perpendicular to the first and the third plurality of spaced apart conductors.

400. The method of claim 391, further comprising monolithically forming a plurality of additional device levels of the array to form a three dimensional monolithic array having at least three device levels.

401. A flash memory array disposed above a substrate, the array comprising:

a first plurality of spaced-apart conductive bit lines disposed at a first height above the substrate in a first direction; and

a second plurality of spaced-apart rail-stacks disposed at a second height in a second direction different from the first direction, each rail-stack including:

a plurality of semiconductor islands whose first surface is in contact with said first plurality of spaced-apart conductive bit lines;

a conductive word line; and

charge storage regions disposed between a second surface of the semiconductor islands and the word line.

402. The array of claim 401, wherein said semiconductor islands comprise polysilicon of a first conductivity type.

403. The array of claim 402, wherein said polysilicon islands include outdiffusion source and drain regions of a second conductivity type at contacting intersections between said spaced-apart conductive bit lines and said spaced-apart rail-stacks.

404. The array of claim 403, wherein said spaced-apart conductive bit lines comprise polysilicon of the second conductivity type in contact with the source and drain regions.

405. The array of claim 404, further comprising a metal or a metal silicide layer in contact with the bit lines.

406. The array of claim 401, wherein a space between said spaced-apart conductive bit lines contains a planarized insulating material.

407. The array of claim 406, wherein the charge storage regions comprise a dielectric isolated floating gate, electrically isolated nanocrystals or an O-N-O dielectric stack.

408. The array of claim 407, wherein:

the charge storage regions comprise a floating gate between a tunnel dielectric and a control gate dielectric;

lateral sides of the tunnel dielectric and the floating gate are aligned to lateral sides of the semiconductor islands; and

the control gate dielectric extends between the semiconductor islands and contacts the planarized insulating material between the semiconductor islands.

409. The array of claim 407, wherein the charge storage region comprises a floating gate made from hemispherical grain polysilicon with a textured surface located between a tunnel dielectric and a control gate dielectric.

410. The array of claim 401, wherein the word line comprises a polysilicon layer of a second conductivity type and a metal or a metal silicide layer in contact with the polysilicon layer.

411. The array of claim 401, wherein the rail stacks are disposed above the bit lines.

412. The array of claim 401, wherein the rail stacks are disposed below the bit lines.

413. The array of claim 401, wherein the word line and the charge storage region are offset apart from drain regions in the semiconductor islands.

414. The array of claim 413, wherein an insulating layer is located between the semiconductor islands and the word lines in an offset region.

415. The array of claim 401, wherein the semiconductor islands are located at an intersection of the rail stacks and the bit lines.

416. The array of claim 415, wherein TFT EEPROMs are formed at the intersections of the rail stacks and the bit lines.

417. The array of claim 416, further comprising access transistors located at the intersections of the rail stacks and bit lines.

418. The array of claim 417, wherein:

the semiconductor islands contain adjacent channel regions of the access transistor and the EEPROM between common source and drain regions;

the word lines form control gates of the EEPROMs and gate electrodes of the access transistors;

a first insulating layer forms a common control gate dielectric of the EEPROMs and a gate insulating layer of the access transistors; and

a floating gate and a tunnel dielectric are located between the word lines and the channel region of the EEPROMs.

419. The array of claim 416, wherein an EEPROM cell in the array is programmed when its source bit line is grounded, its drain bit line either floats or is grounded, and a high positive voltage pulse is applied to the selected EEPROM cell's word line, while all other bit lines on a same device level are left floating or are placed at a slight positive voltage while all other word lines on the same device level are grounded.

420. The array of claim 419, wherein a plurality of EEPROM cells are programmed at the same time.

421. The array of claim 420, wherein the programming voltage is 10 to 20 V .

422. The array of claim 419, wherein:

an EEPROM cell in the array is erased by pulsing its word line to a high negative value while its source and drain bit lines are grounded; or

an EEPROM cell in the array is erased by grounding its wordline and pulsing at least one of its source and drain to a high positive value.

423. The array of claim 422, wherein:

a plurality of EEPROM cells in the array are erased at the same time by pulsing a plurality of word lines to a high negative value while all bit lines are grounded; or

a plurality of EEPROM cells in the array are erased at the same time by grounding their wordlines and pulsing at least one of their source and drain to a high positive value.

424. A monolithic three dimensional array comprising a plurality of device levels wherein each device level contains the array of claim 415.

425. The array of claim 424, wherein each cell size per bit in the array is about $8F^2/N$ to about $11F^2/N$, where F is a minimum feature size and N is a number of device levels in the array.

426. The array of claim 424, further comprising:

an interlayer insulating layer above the second plurality of spaced-apart rail-stacks;

a third plurality of spaced-apart conductive bit lines disposed at a third height above the substrate in the first direction; and

a fourth plurality of spaced-apart rail-stacks disposed at a fourth height in the second direction different from the first direction, each rail-stack including:

a plurality of semiconductor islands whose first surface is in contact with said third plurality of spaced-apart bit lines;

a conductive word line; and

charge storage regions disposed between a second surface of the semiconductor islands and the word line.

427. The array of claim 426, further comprising:

an interlayer insulating layer above the fourth plurality of spaced-apart rail-stacks;

a fifth plurality of spaced-apart conductive bit lines disposed at a fifth height above the interlayer insulating layer in the first direction; and

a sixth plurality of spaced-apart rail-stacks disposed at a sixth height in the second direction different from the first direction, each rail-stack including:

a plurality of semiconductor islands whose first surface is in contact with said fifth plurality of spaced-apart bit lines;

a conductive word line; and

charge storage regions disposed between a second surface of the semiconductor islands and the word line.

428. The array of claim 424, wherein the word line, the charge storage regions and the semiconductor islands of the rail stacks are aligned in a plane perpendicular to the substrate and parallel to a source to drain direction.

429. The array of claim 428, wherein the word line, the charge storage regions and the semiconductor islands of the rail stacks are aligned in

two planes perpendicular to the substrate and parallel to a source to drain direction.

430. A method of making a flash memory array disposed above a substrate, comprising:

forming a first plurality of spaced-apart conductors disposed at a first height above the substrate in a first direction;

forming a first insulating layer located between the first conductors;

forming a stack of layers comprising a first semiconductor layer and a charge storage film;

patterning the stack to form a plurality of first rail stacks comprising a semiconductor rail and a charge storage region rail, having at least one aligned lateral edge;

forming source and drain regions in the semiconductor rails;

forming a second conductive layer; and

patterning the second conductive layer and the first rail stacks to form a plurality of second rail stacks comprising a word line, charge storage region islands and semiconductor islands, wherein the second rail stacks are aligned in a plane perpendicular to the substrate and parallel to a source to drain direction.

431. The method of claim 430, wherein:

the step of forming the first insulating layer located between the first conductors comprises forming the first insulating layer above and between the first conductors and planarizing the first insulating layer to expose the first conductors; and

the step of forming the stack of layers comprises forming the stack of layers on the exposed first conductors and the planarized first insulating layer.

432. The method of claim 431, wherein the step of forming the source and drain regions comprises outdiffusing dopants of a second conductivity type into the semiconductor islands of a first conductivity type from the first plurality of spaced-apart conductors.

433. The method of claim 430, wherein:

the step of forming the first insulating layer comprises forming the first insulating layer on the semiconductor islands of the second rail stack; and

the step of forming the first conductors comprises forming trenches in the first insulating layer, depositing a second conductive layer in the trenches and over the first insulating layer and planarizing the second conductive layer.

434. The method of claim 430 wherein:

the first conductors comprise a polysilicon layer and a metal or metal silicide layer; and

the word line comprises a polysilicon layer and a metal or metal silicide layer.

435. The method of claim 430, wherein said charge storage region islands comprise dielectric isolated floating gates, electrically isolated nanocrystals, or O-N-O dielectric stacks.

436. The method of claim 435, wherein:

the step of forming the stack comprises forming a tunnel dielectric layer and a floating gate layer over the first semiconductor layer; and

the step of patterning the stack comprises forming a photoresist mask over the floating gate layer and etching the stack to form the plurality of first rail stacks comprising semiconductor rails and charge storage region rails comprising tunnel dielectrics and floating gates, the first rail stacks having two aligned lateral edges.

437. The method of claim 436, further comprising forming a control gate dielectric layer over the floating gates of the first rail stacks, wherein the control gate dielectric layer extends beyond the lateral edges of the first rail stacks.

438. The method of claim 437, wherein the step of patterning the second conductive layer and the first rail stacks further comprises patterning the control gate dielectric layer such that the control gate dielectric is disposed between the word lines and the first insulating layer, and wherein the control gate dielectric is aligned in a plane perpendicular to the substrate and parallel to a source to drain direction to the semiconductor islands, the tunnel dielectric, the floating gates and the control gates.

439. The method of claim 435, wherein:

the step of forming the stack comprises forming a tunnel dielectric layer and a floating gate layer over the first semiconductor layer; and

the step of patterning the stack comprises etching the stack to form the plurality of first rail stacks comprising semiconductor rails having a first width and charge storage region rails comprising tunnel dielectrics and floating gates having a second width smaller than the first width;

such that the first rail stacks contain

one aligned lateral edge of the semiconductor rails, the tunnel dielectrics and the floating gates; and

an exposed portion of the semiconductor rails.

440. The method of claim 439, wherein the step of patterning the stack comprises:

forming a first photoresist mask having a first width over the stack;

etching the first semiconductor layer, the tunnel dielectric layer and the floating gate layer using the first photoresist mask;

forming a second photoresist mask having a second width smaller than the first width over the floating gate layer; and

etching the tunnel dielectric layer and the floating gate layer but not the first semiconductor layer using the second photoresist mask.

441. The method of claim 439, wherein the step of patterning the stack comprises:

forming a first photoresist mask having a first width over the stack;

etching the tunnel dielectric layer and the floating gate layer using the first photoresist mask to expose a portion of the first semiconductor layer;

forming a second photoresist mask having a second width larger than the first width over the floating gate layer and over an exposed portion of the first semiconductor layer; and

etching the first semiconductor layer using the second photoresist mask.

442. The method of claim 439, further comprising forming a control gate dielectric layer over the floating gates and over the exposed portions of the semiconductor rails of the first rail stacks, wherein the control gate dielectric layer functions as a gate dielectric of access transistors over the exposed portions of the semiconductor rails.

443. The method of claim 442, wherein the control gate dielectric layer extends beyond the lateral edges of the first rail stacks.

444. The method of claim 443, wherein the step of patterning the second conductive layer and the first rail stacks further comprises patterning the control gate dielectric layer such that the control gate dielectric is disposed between the word lines and the first insulating layer, and wherein the control gate dielectric is aligned in a plane perpendicular to the substrate and parallel to a source to drain direction to the semiconductor islands, the tunnel dielectric and the control gates.

445. The method of claim 439, further comprising forming a second insulating layer between an exposed portion of the semiconductor rails and the word line to form an offset region.

446. The method of claim 445, further comprising forming the second insulating layer between the semiconductor rails to isolate the semiconductor rails.

447. The method of claim 430, further comprising monolithically forming a plurality of additional device levels of the array to form a three dimensional monolithic array having at least three device levels.

448. The method of claim 447, further comprising forming an interlayer insulating layer between each device level.

449. A charge storage device disposed above a substrate, comprising:

a first layer of transition metal-crystallized silicon disposed above a substrate;

a p-n junction disposed in said first layer; and

a local charge storage film disposed adjacent to said first layer.

450. A monolithic three dimensional array comprising a plurality of device levels containing the devices of claim 449, in which the p-n junction comprises a junction between a source region and a channel or a drain region and a channel.

451. A memory array disposed above a substrate, the array comprising:

a first plurality of spaced-apart conductors disposed at a first height above the substrate in a first direction; and

a second plurality of spaced-apart rail-stacks disposed at a second height in a second direction different from the first direction, each rail-stack including:

a semiconductor film of a first conductivity type in contact with said first plurality of spaced-apart conductors;

a local charge storage film disposed adjacent to the semiconductor film; and

a conductive film disposed adjacent to the local charge storage film,

each said semiconductor film being at least partially crystallized using a transition metal induced lateral crystallization process.

452. A method for manufacturing a charge storage device, comprising:

providing a first amorphous silicon or polysilicon layer above a substrate;

providing a transition metal catalyst into the first layer;

crystallizing the first layer;

forming a p-n junction in said first layer; and

forming a local charge storage film disposed adjacent to said first layer.

453. The method of claim 452, wherein the crystallizing occurs at a temperature in a range of about 400°C to about 700°C, and further comprising further crystallizing said first layer with a high-temperature anneal in a range of about 750°C to about 975°C.

454. The method of claim 452, further comprising forming a gate disposed adjacent to the local charge storage film.

455. The method of claim 454, further comprising forming a plurality of device levels comprising transition metal-crystallized silicon TFTs.

456. A semiconductor device comprising a monolithic three dimensional array of charge storage devices comprising a plurality of device levels, wherein at least one surface between two successive device levels is planarized by chemical mechanical polishing.

457. The semiconductor device of claim 456, wherein the array contains four or more device levels.

458. The semiconductor device of claim 457, wherein each charge storage device comprises a pillar TFT EEPROM.

459. The semiconductor device of claim 457, wherein each charge storage device comprises a pillar diode with a charge storage region.

460. The semiconductor device of claim 457, wherein each charge storage device comprises a self aligned TFT EEPROM.

461. The semiconductor device of claim 457, wherein each charge storage device comprises a rail stack TFT EEPROM.

462. The semiconductor device of claim 457, wherein the surface of an insulating or a conductive layer in each device level is planarized by chemical mechanical polishing.

463. The semiconductor device of claim 457, wherein the surface of an interlayer insulating layer located between two levels is planarized by chemical mechanical polishing.

464. The semiconductor device of claim 457, wherein a peak to peak roughness of the surface planarized by chemical mechanical polishing is 4000 Angstroms or less.

465. The semiconductor device of claim 457, further comprising driver circuitry formed in the substrate at least in part under the array, within the array or above the array.

466. The semiconductor device of claim 465, wherein the driver circuitry comprises at least one of sense amps and charge pumps formed under the array in the substrate.

467. A method of making a monolithic three dimensional array of charge storage devices comprising:

forming a plurality of device levels; and

planarizing at least one surface between two successive device levels by chemical mechanical polishing.

468. The method of claim 467, further comprising:

forming four or more device levels; and

planarizing at least one surface between at least three successive device levels by chemical mechanical polishing.

469. The method of claim 468, wherein each charge storage device is selected from a group consisting of a pillar TFT EEPROM, a pillar diode with a charge storage region, a self aligned TFT EEPROM, and a rail stack TFT EEPROM.

470. The method of claim 468, wherein a surface of an insulating layer in each device level is planarized by chemical mechanical polishing.

471. The method of claim 468, wherein a surface of a conductive layer in each device level is planarized by chemical mechanical polishing.

472. The method of claim 468, wherein the surface of an interlayer insulating layer located between two levels is planarized by chemical mechanical polishing.

473. The method of claim 468, further comprising forming driver circuitry in a substrate at least in part under the array, within the array or above the array.

474. The method of claim 473, wherein the driver circuitry comprises at least one of sense amps and charge pumps formed under the array in the substrate.

475. A semiconductor device comprising a monolithic three dimensional array of charge storage devices comprising a plurality of device

levels, wherein at least one surface between two successive device levels has a peak to peak roughness of 4000 Angstroms or less within a stepper field.

476. The semiconductor device of claim 475, wherein the array contains four or more device levels.

477. The semiconductor device of claim 476, wherein each charge storage device comprises at least one of a pillar TFT EEPROM, a pillar diode with a charge storage region, a self aligned TFT EEPROM and a rail stack TFT EEPROM.

478. The semiconductor device of claim 475, wherein the at least one surface between two successive device levels has a peak to peak roughness of 500 to 1000 Angstroms within a stepper field.

479. The semiconductor device of claim 478, wherein the at least one surface comprises a surface of an insulating or a conductive layer in each device level that is planarized by chemical mechanical polishing.

480. The semiconductor device of claim 478, wherein the at least one surface comprises a surface of an interlayer insulating layer located between two levels that is planarized by chemical mechanical polishing.

481. The semiconductor device of claim 475, further comprising driver circuitry formed in the substrate at least in part under the array, within the array or above the array.

482. The semiconductor device of claim 481, wherein the driver circuitry comprises at least one of sense amps and charge pumps formed under the array in the substrate.